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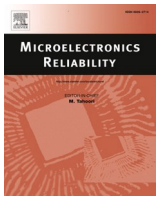

Research Paper

Gate lifetime investigation at low temperature for p-GaN HEMT☆

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ABSTRACT

This paper investigates the time-dependent gate degradation of Schottky-type p-GaN gate transistors by the application of constant electrical stress until the breakdown of the device, indicated by a sudden increase in the gate leakage current. Tests are performed at voltage levels outside the datasheet limits to accelerate the occurrence of failure. To understand the impact of temperature on the failure mechanism, tests encompass temperature ranges from −55 °C to 80 °C, within datasheet recommendations. Results demonstrate that the lower the temperature, the shorter the lifetime, indicating a negative activation energy. Results also present a non-constant activation energy within the range of tested temperatures, demonstrating a complex temperature dependence of the failure mechanism that might not be unique over this temperature range. A very low lifetime of only one day was estimated at −55 °C at the nominal datasheet voltage. The validity of the projection was experimentally confirmed. This underlines the importance of further investigating the gate behavior at low temperatures, as it could be critical for certain applications. Additionally, this challenges the standard gate reliability tests typically performed at the maximum temperature rating of the device, which do not appear to represent the worst-case condition for the gate lifetime.

1. Introduction

High electron mobility transistor HEMT, utilizing p-GaN technology, exhibits favorable physical characteristics, particularly for high-frequency and power applications [1,2]. Nevertheless, there are some concerns regarding their reliability, robustness, and stability. Given the relatively recent emergence and intrinsic differences of GaN technology compared to its more mature Si and SiC counterparts, it is important to recognize that the physics of failure may not be the same [3]. Thus, comprehensive studies are required to discern these distinctions and potentially adapt qualification tests accordingly.

Gate lifetime is a crucial aspect for *E*-mode Schottky p-gate (SP-HEMT) reliability. However, the literature is quite limited on this subject. Usually, gate lifetime is investigated using accelerated tests, where the voltage is used as a stressor to accelerate the failures occurrence. By employing fitting models, lifetime is then estimated for nominal usage conditions. Despite certain number of studies existing on the subject, suggesting that SP-HEMTs exhibit a negative activation energy [4–6], very limited research exists on measurements performed at low temperatures (< 0 °C) [4]. This makes it challenging to predict lifetime in this temperature range or confirm whether the same failure mechanisms apply at low and high temperatures.

This can be problematic, as transistor behaviour at low temperatures can be critical for specific applications. Additionally, the qualification is realized at high temperatures, which may not necessarily be sufficient, as it might not represent the worst-case scenario for HEMTs. Therefore, expanding research efforts to encompass cold temperatures is crucial for a comprehensive understanding of the device's performance spectrum and ensuring its reliability across various operating environments.

The device under study is a commercial Schottky p-GaN HEMT, with its electrical parameters presented in Table 1. The first part of the article focuses on step stress measurements, which were used to determine both the breakdown voltage and the temperature influence. The second part is dedicated to the gate lifetime investigation under static stress; a

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Table 1
Different electrical parameters of the Device under Test.

Parameter	Value
V_{DS} max	650 V
R_{dson}	50 mΩ
I_{dmax}	30 A
V_{GS} min/max	−10 V/7 V

comprehensive study is presented, assessing both temperature and voltage influence on the devices failing behaviour.

2. Test bench

To perform the step stress and gate lifetime tests, a test bench has been developed to apply the stress on the gate Device Under Test (DUT). With this setup, the gate voltage can be applied in two modes: either incrementally increasing in steps (step stress mode) or maintained at a constant level (continuous mode). In both cases, drain and source are shorted to the ground. A schematic of the used circuit is shown in Fig. 1, showing the stress signal for the continuous mode. Current is monitored individually for each DUT throughout the tests. Three bias boards are used, each with 10 individual positions, allowing testing three different bias conditions (one per board) at the same time (see Fig. 2).

3. Preliminary investigation: Step stress

Initially, before starting the static stress, a step stress assessment was performed to determine the gate breakdown-voltage at various temperatures allowing a more informed formulation of the test plan for the static gate lifetime evaluation. In the step-stress test, the gate voltage (V_{GS}) was incremented, starting with V_{GS} = 7 V, by 2 min steps and increasing by 0.2 V, until the gate breakdown was observed. The breakdown is indicated by a sudden increase in the leakage current.

Fig. 3 presents an example of a step stress result, performed at 25 °C. The figure shows the voltage (blue) staircase line and the gate leakage current (red line) at the same time. In this case, the breakdown is observed at 3000 s, which corresponds to V_{GS} = 9.5 V.

The step stress was performed at different temperatures (−55 °C, 25 °C, and 80 °C), with 10 components per condition. Fig. 4 presents the breakdown voltage (V_{BR}) found at various temperatures, illustrating that V_{BR} evolves by increasing the test temperature. This suggests that the gate robustness diminishes at colder temperatures.

4. Gate lifetime investigation

In this section, the lifetime of p-GaN is investigated by performing static stress tests at different temperatures and voltages to understand the impact of each stressor on the device lifetime.

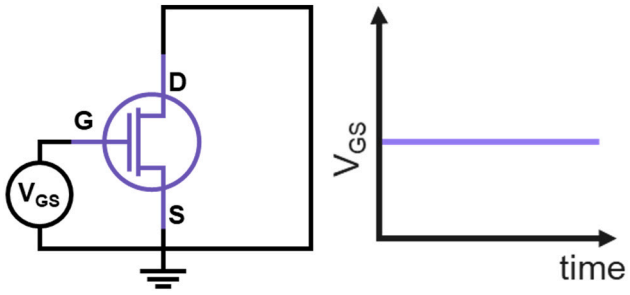

Fig. 1. Schematic of the tetsing circuit (left) and stress waveform for the continuous mode (right).

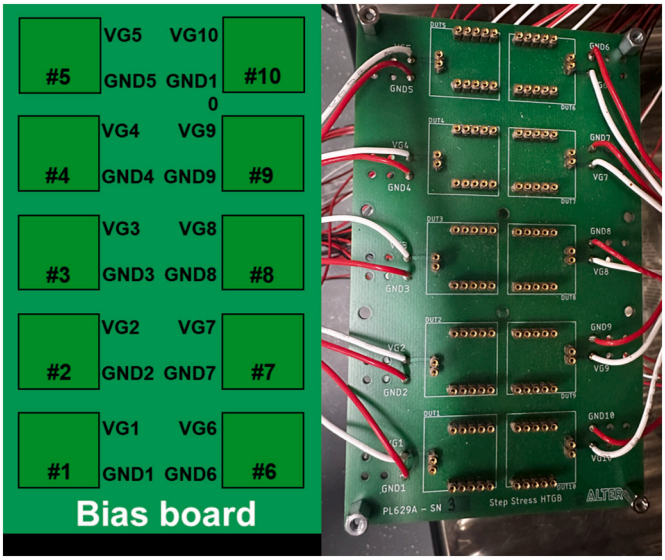

Fig. 2. Bias board (Left: theorical) (right: real).

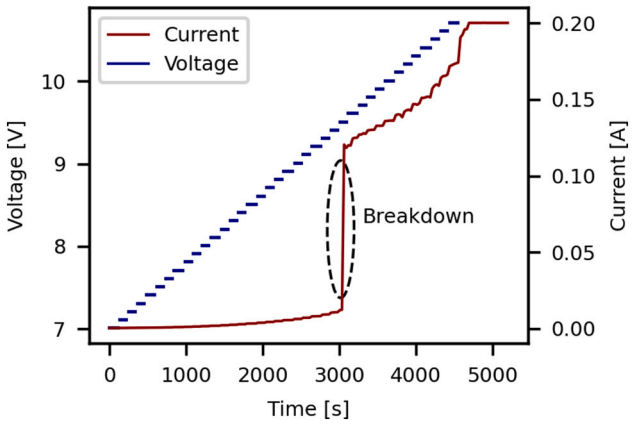

Fig. 3. Step-stress results at 25 °C on one component. The blue staircase line is the voltage, and the continuous red line is the current. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

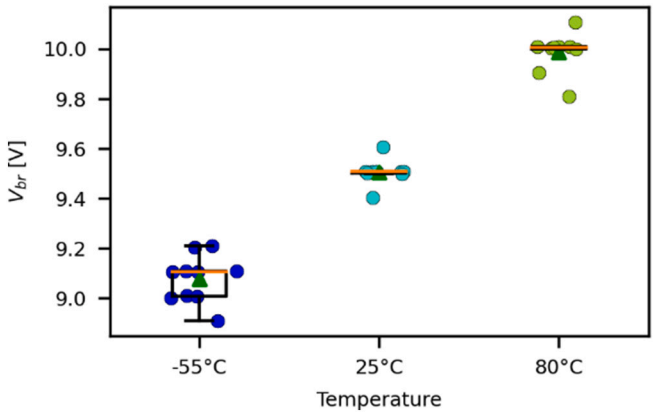

Fig. 4. Breakdown voltages measured at different temperatures, with the green triangle present the mean breakdown. The lower the temperature the lower the V_{BR}. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

4.1. Design of experiment

In this part, the Design of Experiments (DOE) for static stress is presented. The test consisted of applying a static positive gate voltage while keeping the drain and the source shorted to the ground. The gate current (I_G) was continuously monitored until the device failures occurred, to determine the exact failure time of each device. The DOE is represented in Table 2.

From the step-stress test presented in the previous section, it was evident that lower temperatures corresponded to shorter lifetimes. To confirm this observation, static tests were performed across four different temperatures: -55 °C, −15 °C, 25 °C, and 80 °C and with the same voltage on the gate at 9 V.

Furthermore, to assess the impact of voltage, accelerated tests were performed at various voltage levels at the lowest temperature allowed by the datasheet. This permitted the extrapolation of gate lifetime under the nominal voltage. For a meaningful statistical analysis, 10 DUTs were tested under each condition.

The proposed stress in this study was conducted at $V_{GS} > V_{th}$ and $I_{DS} = 0$ A to isolate and directly analyse the degradation mechanisms of the gate under controlled conditions. This approach allows us to focus specifically on the behavior of the gate itself, without the influence of additional degradation modes that might occur under operational conditions ($V_{GS} > V_{th}$, $I_{DS} > 0$). While this setup may not fully replicate practical application conditions, it provides valuable insights into the intrinsic reliability of the gate. In addition it allows us to understand if the classical HTGB qualification tests are suitable to the GaN HEMT technology or if they requires modifications.

4.2. Temperature-dependent gate lifetime

As described in the DOE section, a study was conducted on the influence of temperature on the gate lifetime. The applied gate voltage was 9 V, and tests were conducted at −55 °C, −15 °C, 25 °C and 80 °C.

An example of the result is shown in Fig. 5, where the measured I_G over time for $V_{GS} = 9$ V and T = -55 °C is reported for 10 DUTs. As expected, a similar behavior was observed for the other conditions. As for the step-stress test, failure time was considered as the time at which the gate leakage current increases abruptly.

The same measurements were conducted also at −15 °C, 25 °C, and 80 °C at 9 V. Results are shown with the Weibull plots reported in Fig. 6. It can be noticed that, for all the conditions, the Weibull plots are parallel. The shape parameter β values are: 2.79 at −55 °C, 2.70 at −15 °C, 2.88 at 25 °C and 2.56 at 80 °C. This parallelism indicates that the failure mechanism remains consistent across this temperature range. At −55 °C, the mean time to failure (MTTF) is the shortest, indicating a rapid degradation of the gate under constant electrical stress at this temperature. As the temperature increases, a corresponding increase in lifetime is observed, with progressively higher MTTF values at −15 °C, 25 °C, and finally 80 °C, where the robustness of the p-GaN gate is significantly enhanced. This confirms the lower robustness of the p-GaN gate at low temperatures, where the failure mechanism appears to be more accelerated, while at higher temperatures, the devices show greater lifetime under stress.

Table 2
Design of Experiment for gate lifetime stress under different temperatures and V_{GS} voltage stress.

Condition #	Temperature	V_{GS} voltage
1	-55 °C	7 V
2	− 55 °C	8 V
3	− 55 °C	8.5 V
4	− 55 °C	9 V
5	−15 °C	9 V
6	25 °C	9 V
7	80 °C	9 V

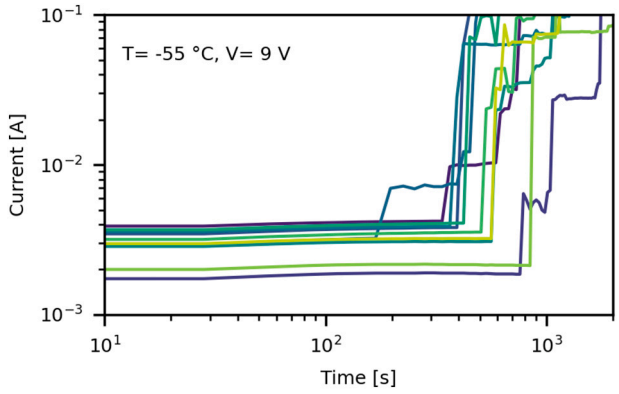

Fig. 5. Example of gate bias stress on 10 DUTs at −55 °C, 9 V, which all present failures.

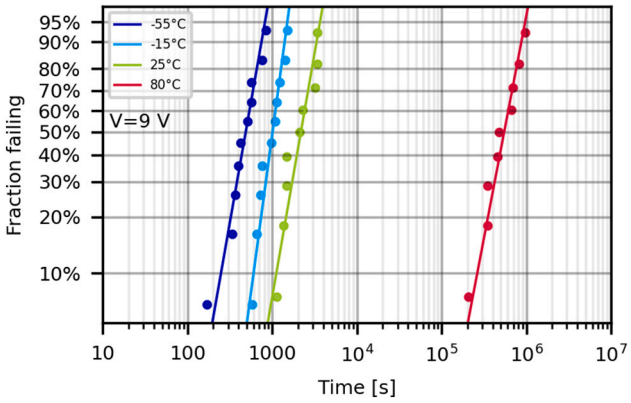

Fig. 6. A Weibull plot of time to failure at −55 °C, −15 °C, 25 °C and 80 °C with $V_{GS} = 9$ V, which exhibits smaller TTFs at cold temperatures.

Fig. 7 displays the Time to Failure (TTF) for fraction failing equal to 63 % as a function of temperature (1000/T), allowing the calculation of the activation energy (E_A) using the Arrhenius model described by the following equation:

$$MTTF = A.e^{\frac{E_A}{KT}}$$

It is noticeable that there are two distinct activation energies (E_A = -0.9 eV between 80 °C and 25 °C, and E_A = −0.1 eV between 25 °C, −15 °C and − 55 °C), suggesting that a traditional Arrhenius model cannot accurately describe the temperature dependence across this

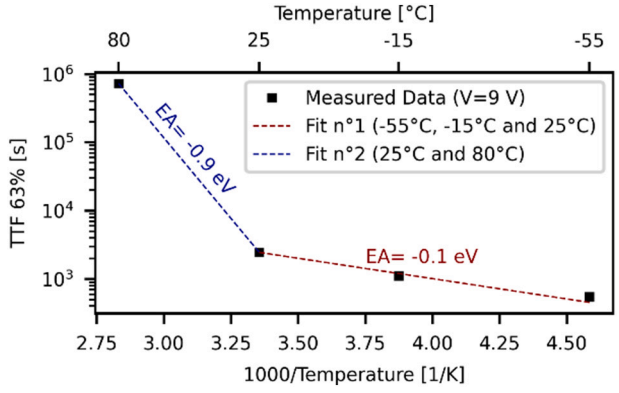

Fig. 7. Arrhenius plot of TTF at 63 % with $V_{GS} = 9$ V showing two activation energies (E_A), demonstrating a complex temperature dependence of the failure mechanism.

range. Further investigation is necessary to develop a more precise model. It is important to mention that the E_A calculated between 25 °C and 80 °C is only indicative, as at least one additional measurement point is desirable to better estimate its value. At temperatures below 25 °C, even with a negative activation energy, the TTF decreases with a lower slope compared to the range between 25 °C and 80 °C. Therefore, the acceleration is slower with lower temperature dependence.

4.3. Voltage-dependent gate lifetime

After understanding the influence of temperature on the gate lifetime and identifying cold temperatures as the worst-case scenario, a focus was directed towards cold temperature conditions. Measurements were conducted at −55 °C to investigate the impact of the applied stress voltage and to project the results at 7 V, which is the maximum rating according to the datasheet.

Measurements were taken for $V_{GS} = 8$ V, 8.5 V, and 9 V to accelerate the failure mechanism and estimate the lifetime at given voltages. Fig. 8 presents the results in Weibull distribution, indicating very low TTFs at −55 °C. When the projection was conducted using the exponential model at V_{GS} = 7 V (max rating), a TTF of approximately 20 h was obtained.

To confirm the validity of the theoretical projection and to ensure that the same mechanism exists between 9 V and 7 V, additional measurements were carried out at 7 V. The green dots in Fig. 8 illustrates the experimental results, which closely match the projected curve (indicated by the dotted red line). The projection was obtained by using the exponential model (TTF ~ exp.[−α/V]). Fig. 9 illustrates the TTF for 63 % fraction failing as a function of the voltage V_{GS}. Two fitting models, both present in the literature, were employed to estimate the lifetime: (i) the exponential model V^{-1} where TTF ~ exp.(α/V) [7–9] and the (ii) exponential $V^{1/2}$ which is based on the assumption that the gate leakage current is dominated by Poole–Frenkel (PF) emission [4]. Both models indicate that to achieve, for example, a lifetime of 10 years, applying a voltage lower than the datasheet's specification is required. Specifically, according to the exponential model V^{-1}, the most optimistic results suggest applying 5.1 V, while the exponential $V^{1/2}$ suggests 4.5 V.

5. Physical explanation

In this section, a physical explanation of the different failure mechanisms occurring during a gate lifetime test will be provided in detail. Various degradation processes contribute to the breakdown of the gate structure in p-GaN HEMTs under gate stress. According to the literature, gate breakdown is likely caused by the formation of defect levels in the gate area. Fig. 10 provides a simplified cross-sectional view of a p-GaN HEMT, along with a schematic band diagram of the metal/p-GaN/

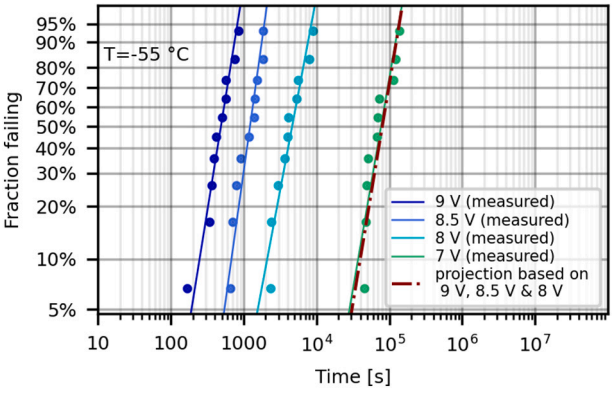

Fig. 8. A Weibull plot illustrating the time to failure at −55 °C for different V_{GS} values (full lines) 8 V, 8.5 V, and 9 V. Projection based on experimental data is included, demonstrating its alignment with the measured data at 7 V.

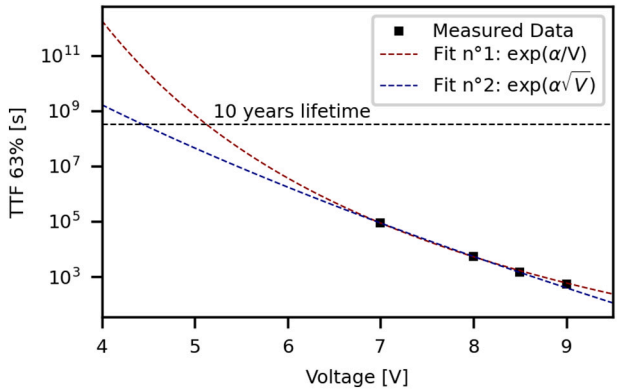

Fig. 9. Lifetime prediction with exponential V^{-1} and exponential $V_{1/2}$ at −55 °C. Projections indicate that to achieve a lifetime of 10 years a lower voltage than the maximum datasheet's specification is required.

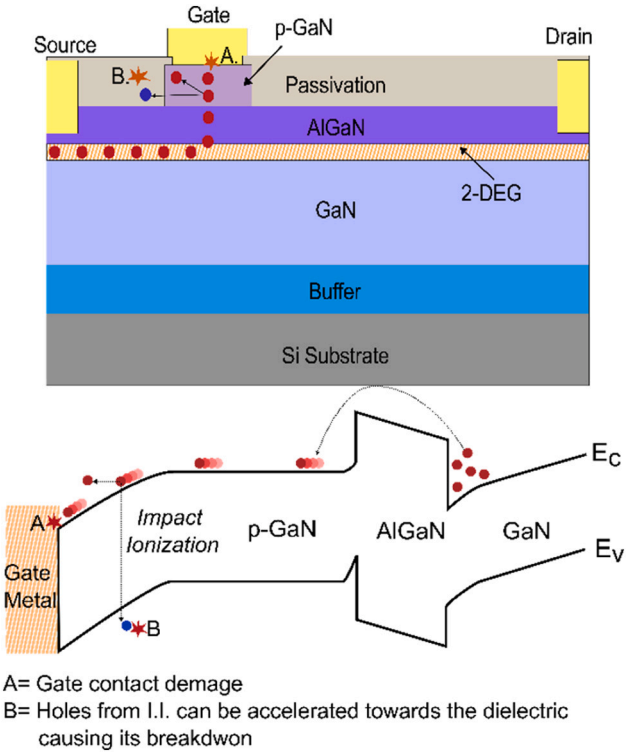

Fig. 10. Simplified cross section of p-GaN HEMT. And a schematic band diagram of the metal/p-GaN/AlGaN/GaN gate stack, showing the two main failure mechanisms during gate lifetime test.

AlGaN/GaN gate stack. This gate stack structure can be modeled as two diodes in series: a reverse-biased metal/p-GaN Schottky junction and a forward-biased p-i-n heterojunction.

Indeed, under positive gate stress, the reverse-biased metal/p-GaN Schottky junction and forward-biased p-i-n heterojunction lead to electron and hole injections into the p-GaN layer, where a high electric field is present, generating highly energetic carriers. These carriers cause two failure mechanisms: first, degradation of the Schottky contact, and second, impact ionization, which results in Si_3N_4 dielectric breakdown near the p-GaN region. These two phenomena will be detailed in the next sections.

5.1. Schottky contact degradation

One of the possible sources of failure is linked to the metal/p-GaN

contact. As per [5,10], under positive gate stress, electrons in the 2-DEG channel can overflow the AlGaN barrier and be injected into the p-GaN layer. In the depleted p-GaN region, where a strong electric field is present, these carriers (electrons and holes) are accelerated and gain high energy. As a result, high-energy electrons bombard the metal/p-GaN interface or the nearby p-GaN layer, creating defect levels. With accumulated stress, a sufficient defect concentration builds up, transforming the gate contact from Schottky-type to an Ohmic-like contact, ultimately leading to gate breakdown. The negative activation energy can be explained by stronger lattice scattering at higher temperatures, which reduces carrier mobility and accelerates defect formation at elevated temperatures.

5.2. Impact ionization

Another potential failure mechanism is related to impact ionization. In [6,11] the authors hypothesize that the breakdown could be linked to impact ionization, which is indeed a phenomenon more likely to occur at lower temperatures. According to the authors, once electrons are accelerated within the depleted region, they can gain enough energy to cause impact ionization and generate electron-hole pairs, particularly in the region with a high electric field. After that, holes could move away, and a certain number of holes could be trapped in the Si_3N_4 passivation dielectric. The accumulation of these trapped charges increases the electric field within the dielectric, and once a critical charge density is reached, it can cause dielectric rupture, leading to catastrophic damage at the sidewall between the p-GaN and the Si_3N_4.

6. Conclusion

In conclusion, accelerated lifetime tests of the gate were conducted on a commercial SP-HEMT, studying the influence of temperature and voltage on the gate's lifetime. Measurements at 9 V were performed at different temperatures (−55 °C, −15 °C, 25 °C, and 80 °C), revealing that the lower the temperature, the shorter the lifetime. Additionally, it was demonstrated that the activation energy is negative, and not constant between −55 °C and 80 °C. For $T < 25$ °C the TTF dependency on temperature is lower than $T > 25$ °C.

Given that cold temperatures represent the worst-case scenario, a focus was directed towards

-55 °C to investigate the influence of applied stress voltage on lifetime and to project results to nominal voltages. The results showed a TTF of approximately 20h at 7 V, suggesting that to achieve a TTF of 10 years, the applied voltage should not exceed 5 V.

Finally, the results of this study emphasize the importance of revising the qualification protocols for GaN-based transistors. Currently, traditional JEDEC JESD92 [12] protocols focus on qualifying the gate through the High-Temperature Gate Bias (HTGB) tests, where the applied temperature is the maximum allowed by the datasheet. However, given the criticality of gate lifetime at low temperatures, it is evident that HTGB tests need to be complemented with tests performed at room temperature or below, as this represents the most severe condition for the device and ensuring correct qualification is essential for reliability across various operating conditions.

CRediT authorship contribution statement

M. Alam: Writing – original draft, Investigation, Formal analysis, Conceptualization, Methodology. **V. Rustichelli:** Writing – review & editing, Formal analysis, Conceptualization, Methodology. **M. Zerarka:** Writing – review & editing. **C. Banc:** Writing – review & editing. **J. Pieprzyk:** Writing – review & editing. **O. Perrotin:** Investigation, Writing – review & editing. **R. Ceccarelli:** Investigation, Writing – review & editing. **D. Trémouilles:** Formal analysis, Writing – review & editing, Methodology. **M. Matmat:** Supervision, Writing – review & editing. **F. Coccetti:** Project administration, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The data that has been used is confidential.

References

[1] R. Sun, J. Lai, W. Chen, B. Zhang, GaN power integration for high frequency and high efficiency power applications: a review, IEEE Access 8 (2020) 15529–15542.
[2] M. Haziq, S. Falina, A. A. Manaf, and H. Kawarada, "Challenges and opportunities for high-power and high-frequency AlGaN/GaN high-Electron-mobility transistor (HEMT) Applications : A Review," 2022.
[3] J.P. Kozak, et al., Stability, reliability, and robustness of GaN power devices: a review, IEEE Trans. Power Electron. 38 (7) (2023) 8442–8471.
[4] J. He, et al., Low-temperature accelerated gate reliability of Schottky-type p-GaN gate HEMTs, Proc. Int. Symp. Power Semicond. Devices ICs 2020–Septe (2020) 290–293.
[5] J. He, J. Wei, S. Yang, M. Hua, K. Zhong, K.J. Chen, Temperature-Dependent Gate Degradation of p-GaN Gate HEMTs under Static and Dynamic Positive Gate Stress, 2019 31st international symposium on power semiconductor devices and ICs (ISPSD) 1 (2019) 295–298.
[6] S. Zhang, et al., Projecting GaN HEMTs lifetimes under typical stresses commonly observed in DC-DC converters, Power Electron. Devices Components 6, no. August (2023) 100051.
[7] M. Abouie, GaN Systems Demonstrates Reliability Based on Qualification and Lifetime Data, in: Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, 2020, p. 14.
[8] I. Rossetto, et al., Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate, IEEE Trans. Electron Devices 63 (6) (2016) 2334–2339.
[9] A.N. Tallarico, et al., Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs, IEEE Electron Device Lett. 38 (1) (2017) 99–102.
[10] H. Gao, A. Espinoza, R. Garcia, S. Gajare, S. Zhang, Main mechanism responsible for pGaN gate breakdown and lifetime projection in GaN HEMTs, IEEE Trans. Electron Devices 71 (10) (2024) 5933–5940.
[11] M. Fregolent, et al., Negative activation energy of gate reliability in Schottky-gate p-GaN HEMTs: combined gate leakage current modeling and spectral electroluminescence investigation, IEEE J. Electron Devices Soc. 12 (July) (2024) 703–709.
[12] "Procedure for characterizing time-dependent dielectric breakdown of ultra-thin gate dielectrics: | JEDEC," Accessed on: Sep. 27, 2022." [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-92.