TID Characterization of 24-45nm COTS NAND Flash for Space Applications

B. Tanios, O. Perrotin, B. Forgerit, F. Tilhac, F.X. Guerre, C. Poivey

Abstract— **This work presents a comparative study of Total Ionizing Dose (TID) radiation sensitivity of five COTS (commercial off-the-shelf) 24-45 nm NAND flash memories for space applications.**

Index Terms—**COTS, NAND flash, Total Ionizing Dose.**

I. Introduction

Flash memories are non-volatile memory storage that can be electrically erased and reprogrammed. There are two main types of flash memory named after the NAND and NOR logic gates. With reduced erase and write times and less chip area by cell allowing higher memory density and lower cost per bit than the NOR flash, the NAND flash is highly suitable for mass-storage devices, e.g. memory cards, USB flash drives and solid-state drives.

Actually, NAND flash devices have very large capacity attending 256 Gbits for single level cell (SLC) NAND flash by stacking in the same package several dies of 32 Gbits per die, and even higher densities for multi-level cell (MLC) NAND flash. However, MLC NAND flash is much more radiation sensitive than the SLC NAND flash since it has less margins on stored voltage status detection. Additionally, NAND flash is low power and has good mechanical shock resistance in comparison with traditional hard disks. These good qualities of NAND flash make it suitable for use in space mass-storage systems where it has been considered since Spot-6 launched in 2012 and Sentinel-2 launched in 2013.

The electronic equipment on spacecrafts is potentially exposed to harsh radiation environment, e.g. the ESA JUICE spacecraft, which will be exploring Jupiter and its system, will be exposed to dense population of high energy electrons in Jupiter's radiation belts [1], inducing TID levels in the 200-400 krad range behind 8-10 mm aluminum shielding [2]. Additionally, it will also face the SEE effects induced by solar particles and cosmic rays. Therefore, the TID and SEE behavior of NAND flash under space radiation environment is a key element fo r space missions. The objective of this study is to perform TID radiation characterization tests on three NAND flash memory parts to determine whether they are suitable for space applications.

II. Parts Under Study

An examination of commercial-off-the-shelf NAND flash devices was performed and five memory candidates that could potentially be adopted as storage devices for the mass memory unit for space applications have been selected to perform the TID radiation tests [3]. Criteria of selection included device production status, reported radiation tests in the literature (2016), and die technology. The selected devices main characteristics are summarized in Table 1.

Table 1. NAND Flash Devices Main Characteristics

Manuf.	Part Number	Date code	Pack.	Orga.	Cap.	Access Time	Feat. Size*
Hynix	H27U4G8F2D	1503	TSOP 48	4096 blks x 64 pgs x 2 kB	4 Gb	25 ns	41 nm
Toshiba	TC58NVG2S0HTAI0	1509	TSOP 48	2048 blks x 64 pgs x 4 kB	4 Gb	25 ns	24 nm
Macronix	MX30LF4G18AC-TI	1444	TSOP 48	2 plns x 2048 blks x 64 pgs x 2 kB	4 Gb	20 ns	32 nm
Spansion	S34ML04G200TFI000	1442	TSOP 48	2 plns x 2048 blks x 64 pgs x 2 kB	4 Gb	25 ns	32 nm
Winbond	W29N01GVSIAA	1437	TSOP 48	1024 blks x 64 pgs x 2 kB	1 Gb	25 ns	45 nm

*Feature size is given based on the reverse construction analysis done at Alter Technology France laboratory.

The selected parts have been reversely analyzed [4]. The five parts under review, Hynix, Toshiba, Macronix, Spansion and Winbond, use the same kind of architecture with bit line and ground access transistors for each serial block. The Toshiba technology is the most integrated with minimum node at critical dimension (CD) of 24 nm vs 32 and 45 nm on the other parts. Same observation on cell architecture where Toshiba uses 66 serial cells per block compared to 34 serial cells for the other parts. Winbond memory is a 1 Gb compared to 4 Gb of other

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parts. The process challenge regarding the uniformity of cell definition in the dense matrix seems to be achieved on all part technologies. Small air gaps were only observed at the top of the cell stack on Hynix, Macronix and Spansion technologies.
The control circuitry area constitutes between 26% and 57% of the total die area.

The main challenge for this type of technology is the process capability with the die manufacturing lithography and etching tools. Repeatability of cell spacing Air Gap and minimum Critical Dimension (CD's) patterns definition are most likely the main yield detractors on these parts.

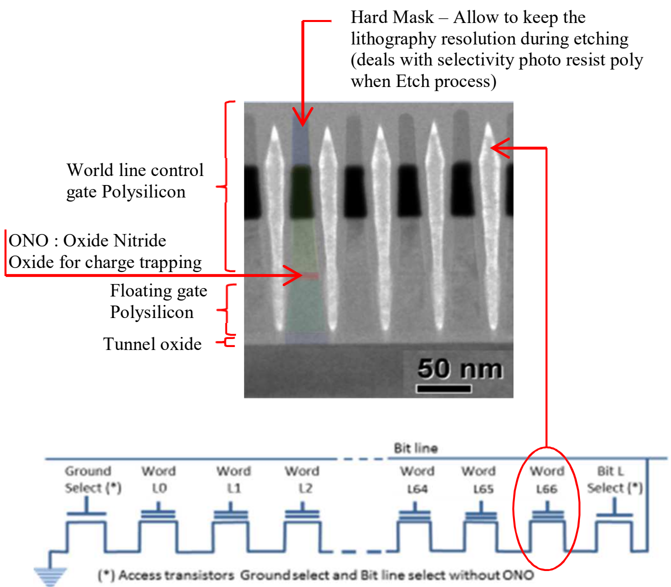

Fig. 1. NAND flash memory cell architecture

III. Test Setup

The in-situ test system (cf. Fig. 2) is based on a control board (STB025C) composed of a PIC32MX processor from Microchip and a Spartan6 FPGA from Xilinx. The devices to be tested (DUTs) are mounted on daughter boards (DIB248C).

The control board includes the biasing and functional checks of the DUTs and can drive up to 20 NAND flash memories in parallel.

The test flow is configured and controlled through a computer graphical user interface (UI). Commands like read, write flash devices are sent by the UI to the controller board which executes these commands and interfaces with the devices under test.
Then, after execution of the command, the control board sends to the UI the results data composed of operation status data (success/fail), error data and log data. These data are then recorded by the UI.

The communication between the control board and the computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.
DUTs power supplying and monitoring is managed by an external power supply.

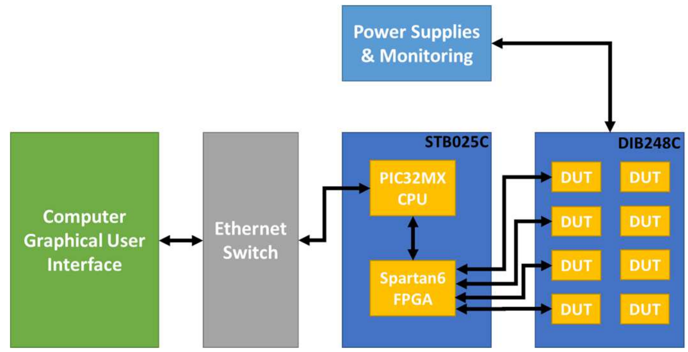

Fig. 2. In-situ Test Setup.

IV. Test Procedure

The DUTs have been irradiated at UCL facility located in Louvain (Belgium) at a dose rate of 300 rad (Si)/h. The irradiator is a Co60 source. The dosimetry has been calibrated using a RADCAL Model 2186 active dosimeter. The dose received by the devices has been controlled by the measurement of one Alanine pellet dosimeter placed onto each bias board.

During the dose exposures, DUTs have been irradiated in an ambient temperature of 24 °C ± 6 °C. During the annealing step at 100 °C ± 5 °C, the temperature was controlled using an external monitoring system.

During exposure and annealing steps, 30 test samples are split into three different sets with 10 devices in each set:
- Set 1: Biased OFF samples (pins connected to ground).
- Set 2: Biased at low duty cycle (LDC) (stand-by with occasional read/erase/program cycles every 1krad(Si)).
- Set 3: Biased at high duty cycle (HDC) (with permanent looping of erase/program/read cycles).

Intermediate parametric electrical measurements have been performed at 0, 30, 50, 150, and 200 kRad(Si) steps and after annealing steps 24 hours at 25 °C and 168 hours at 100 °C.

A. Electrical measurements between radiation steps

Between radiation and annealing steps, several types of parametric and functional parameters are measured and checked under the conditions of the device datasheet using the Mutest Automatic Test Equipment (ATE), which includes:

- DC: Continuity in ESD diodes, Input Leakage Current (ILI), Output Leakage Current (ILO), Output Low Voltage (VOL), Output High Voltage (VOH), Input Low Voltage (VIL), Input High Voltage (VIH).
- Power Supply: Operating Read Current (ICC1), Operating Program Current (ICC2), Operating Erase Current (ICC3), and standby currents (ICC4 & ICC5).
- AC: Program Time (tProg), Block Erase Time (tBers) and all specified read, program and erase dynamic times.
- Functional Tests:
  - Checkerboard pattern: block 0 is erased, write and read with an alternate "0" and "1" pattern, i.e. 55h and AAh.
  - SLC-March pattern: block 0 is erased, write and read with SLC March Algorithm.

- Data Retention (DR) – Biased OFF parts: block 81 is erased and write with alternative groups of "55h" and "AAh" pattern at 0krad, and it is read in the rest of radiation steps. This test gives information about the long-time data retention along the whole radiation campaign. This mimic the usage of the memory as program storage.

B. In-situ measurements during radiation

Several test sequences are performed during radiation exposure and annealing. Test sequences include Erase, Program and Read checking operations.
The test sequence is different between low and high duty cycle operating modes, not only in timing but also in the flow, which are shown in Fig. 3 and Fig. 4. In LDC operating mode, the DUT is in stand-by with occasional read/erase/program cycles every 1krad(Si)) of received dose. On the other hand, in HDC operating mode a permanent looping of erase/program/read cycles are performed on the DUT.
Furthermore, in each operating mode (LDC/HDC), the 1st half of the memory chip (blocks 1 to N/2 -1) is considered for dynamic behaviour (read/write alternatively) while the 2nd half of the chip (blocks N/2 to N-1) is considered for retention behaviour (only read), with N is the number of blocks of the memory (blocks 0 to N-1).
Note that there is one difference between HDC and LDC testing modes concerning the retention blocks N/2 to N-1. In HDC mode, they are rewritten at the beginning of each exposure or annealing step while in LDC mode they are written only one time, at the beginning of test campaign.

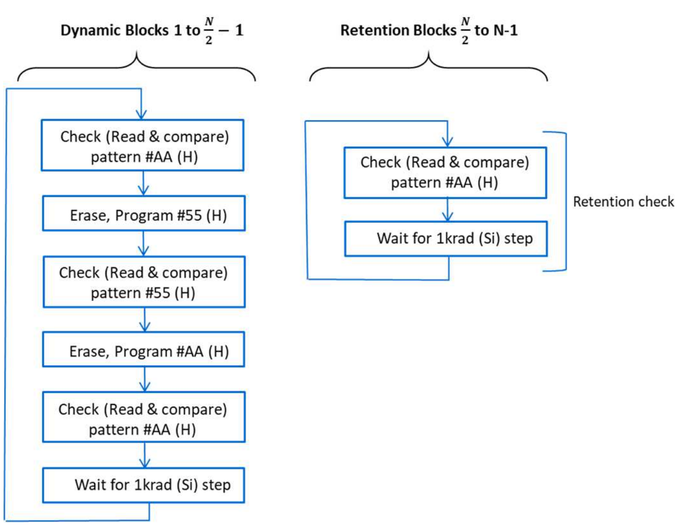

Fig. 3. Low Duty Cycle in-situ test sequence.

The functional parameters recorded by the in-situ test setup are:

- Write errors:
  - Erase failure (E): a block erase failure is stated after 2 failed trials of block erase operation;
  - Program failure (P): a block program failure is stated after 2 failed trials of page program operation;
  - Failed blocks (E+P): a block suffering of erase or program failures.
- Read errors:
  - Blocks with minimum 1 byte in error;
  - Blocks with 90% bytes in error;
  - Total number of bytes in error in the DUT.

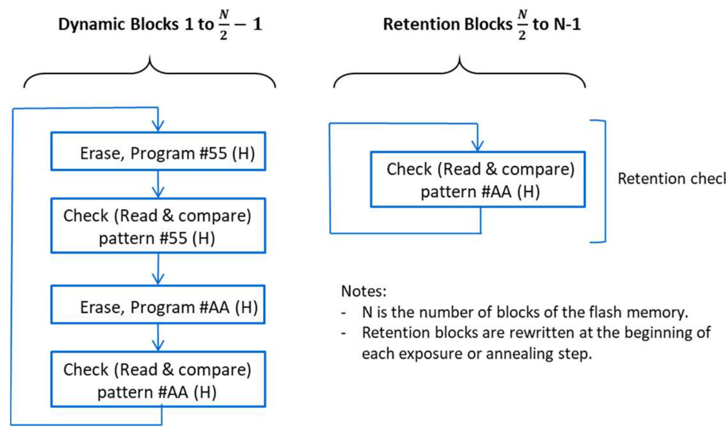

Fig. 4. High Duty Cycle in-situ test sequence.

V. Results

The results of the electrical measurements and in-situ measurements are summarized in
Table 2 and Table 3 respectively.

We observed that much less memory errors occur when ERASE/PROGRAM cycles are implemented periodically in comparison to the READ only test sequence.
For the READ only test, number of errors is related to number of reads (more reads, more errors), i.e. the number of errors is much more important in HDC mode than LDC.

Despite the fact that tested parts technologies are similar, the radiation tolerance across the five NAND flash parts is different. Except Macronix device, all the four other parts have a radiation tolerance dose less than 30 krad(Si). The charge pump block seems to be the critical element for all the memories except Macronix as it's involved in ERASE/PROGRAM operation.

The Macronix part is the one out of the five tested parts that seems the most suitable for space mission at least by considering the TID results.
However, above 100 krad (Si) a catastrophic failure was observed for this part when it is power cycled (off-on): loss of functionality of the device along with power consumption increase.

A 2nd test campaign was done to confirm the influence of the power cycling (power off-on) on device loss of functionality. The samples were kept powered from 0 to 150 krad of total dose. A occasional write operation was executed every about 20 krad, which permitted to recover some memory data errors (cf. jumps-down in number of errors at the beginning of each step in Fig. 5-3.
As it shown in Fig. 5-1, a power overconsumption is observed after the power cycling at the end of exposure. This overconsumption persisted during annealing and no recovery

was observed. Along with the power overconsumption, the devices lost totally their functionality and were not responding.

TABLE 2: ELECTRICAL MEASUREMENTS (MUTEST ATE) RESULTS

Test Parameter	Bias	Part number									
		Winbond		Spansion		Hynix		Toshiba		Macronix	
		Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing
DC	LDC	<30	C	>100	C	<30	P	>200	C	>100*	C
	HDC	<30	C	>100	C	<30	P	>200	C	>100*	C
	OFF	>50	C	>100	C	>100	C	>200	C	>100*	C
Power supply	LDC	<50	C	>100	C	>50	C	>200	C	>100*	C
	HDC	<50	C	>100	C	>50	C	>200	C	>100*	C
	OFF	<50	C	>100	C	>100	C	>200	C	>100*	C
AC timings	LDC	<30	C	<30	N	<30	P	<50	N	>100*	N
	HDC	<30	C	<30	N	<30	P	<50	N	>100*	N
	OFF	>50	C	<100	N	>100	C	<150	C	>100*	N
Functional	LDC	<30	C	<30	N	<30	P	<50	N	>100*	N
	HDC	<30	C	<30	N	<30	P	<30	N	>100*	N
	OFF	>50	C	<100	N	<100	P	<100	P	>100*	N
Data retention	OFF	>50	C	<50	N	<100	N	<50	N	<30	N

*DUTs failed after the power cycling OFF-ON with a cumulated dose > 100krad.

Radiation tolerance :

< symbol indicates that the tested parameter failed at this step.

> symbol indicates that samples finalized their irradiation test at this step (and samples taken to annealing) with the tested parameter is PASS.

Annealing :

C (Complete) indicates that all the samples recovered.

P (Partial) indicates that a least one sample recovered.

N (No) indicates that no sample recovered.

TABLE 3: IN-SITU MEASUREMENTS RESULTS

Test Parameter	Bias	Part number									
		Winbond		Spansion		Hynix		Toshiba		Macronix	
		Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing	Radiation tolerance (krad(Si))	Annealing
Erase/Prog.	LDC	15	N	20	N	25	P	30	N	>150	N
(blks 1 to N/2)	HDC	15	N	20	N	25	P	30	N	>150	N
Read	LDC	15	N	20	N	25	P	30	N	86	N
(blks 1 to N/2)	HDC	15	N	20	N	25	P	30	N	100	N
Read only	LDC	15	P	30	P	30	P	20	N	86	N
(blks N/2 to N-1)	HDC	15	P	30	P	30	P	30	N	86	N

Annealing :

P (Partial) indicates that samples recovered partially (less errors).

N (No) indicates that no sample recovered.

Therefore, power cycling has an impact on total dose radiation tolerance of the Macronix part. Above a total dose of 100 krad (Si) the power cycling of the Macronix device is fatal.

Nevertheless, the Macronix device gived by far the best results in terms of TID in comparison with the four other tested parts.

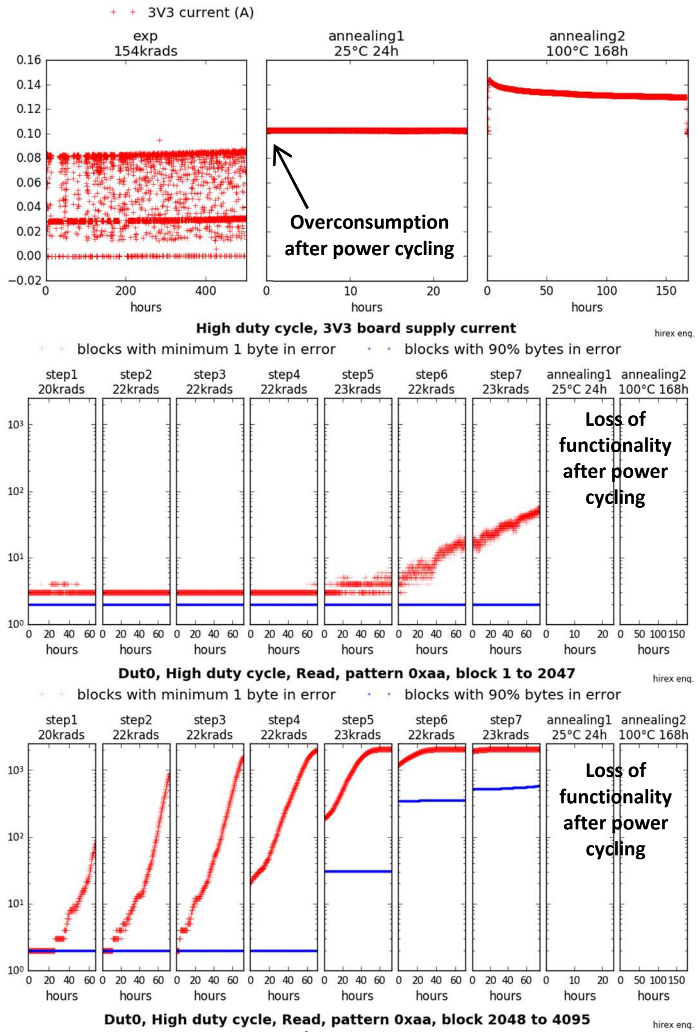

Fig. 5. Macronix 2nd test: In-situ HDC bias results.

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