# Single Event Effects Characterization of 55-65nm NOR Flash for Space Applications

B. Tanios, M. Kaddour, B. Forgerit, F.X. Guerre, C. Poivey

***Abstract*— This work presents a comparative study of Single Event Effects (SEE) radiation sensitivity of two COTS (commercial off-the-shelf) 55-65 nm NOR flash memories for space applications.**

***Index Terms*—COTS, NOR flash, Radiation Effects, Single Event Effects.**

## I. Introduction

Flash memories are non-volatile memory storage that can be electrically erased and reprogrammed. There are two main types of flash memory named after the NAND and NOR logic gates. The NAND flash can be erased in blocks and programmed and read in pages while the NOR flash allows random access, i.e. to write and read independently a single word in the memory, but suffers from long erase and program times. The NOR flash is highly suitable for use with microprocessor as random access ROM since it allows random-access reading with low latency, and has speed and cost advantages over non-flash EEPROM (Electrically Erasable Programmable Read-Only Memory).

As NOR flash has larger capacity than non-flash EEPROM and long retention time, usually 20 years, compared to NAND flash, it makes it highly suitable for long duration space mission to store critical data such as boot code or configuration files. NOR flash has maximal capacity of 1Gb on a single die. Dies may be stacked to obtain larger capacities.

The electronic equipment on spacecrafts is potentially exposed to harsh radiation environment, e.g. the ESA JUICE spacecraft, which will be exploring Jupiter and its system, will be exposed to dense population of high energy electrons in Jupiter's radiation belts [1], inducing TID levels in the 200-400 krad range behind 8-10 mm aluminum shielding [2]. Additionally, it will also face the SEE effects induced by solar particles and cosmic rays. Therefore, the TID and SEE behavior of NOR flash under space radiation environment is a key element for space missions.

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The objective of this study is to perform SEE radiation characterization tests on the NOR flash with 65 nm technology node, selected consequently to the total ionizing dose (TID) tests [3] (TID tolerance ~ 30 krad(Si)), to determine whether they are suitable for space applications.

## II. Parts Selection and Analysis

An examination of commercial-off-the-shelf NOR flash devices was performed and three memory candidates that could potentially be adopted for space applications, e.g. as random access ROM, have been selected to perform the TID radiation tests [4]. Criteria of selection included device production status, reported radiation tests in the literature, and die technology. After the TID tests presented in [3], two parts have been selected for SEE testing. The selected devices main characteristics are summarized in TABLE I.

A technological analysis of the parts has been performed [5]. The selected parts from Macronix and Micron are 1 Gb capacity memories. However, these are fundamentally different in terms of architecture. Macronix is composed of two stacked dice of 40 mm² area compared to Micron with single die of 58 mm². Cell structure of both devices is composed of two serial dual 68nm critical dimension (CD) gate surrounded by two bit lines access transistors. Macronix cell evidences a significant parasitic slope at the top of the control gate due to minimum gate to gate spacing etch which could be considered as the process integration limit.

Additionally, Micron device is multi-level cell (MLC), able to store 2 bits in the same cell while Macronix is single-level cell (SLC) with only one bit per cell.

The cell area of Macronix and Micron is respectively 0.033, 0.039 $\mu m^2$/cell. The control circuitry area constitutes respectively 21% and 29% of the total die area.

## III. SEE Test Setup

The test system (cf. Fig. 1) is based on a Virtex4 FPGA (Xilinx) test board (STB026). The devices to be tested (DUTs) are mounted on daughter boards (DIB294A).
In addition to biasing and functional checks, the test board also includes the voltage/current monitoring and the latch-up

management of the DUT power supplies with up to 24 independent channels. Single event latch-up (SEL) is detected and processed when the supply current is over a configurable threshold. Once detected, SEL state is maintained for typically 2ms (hold time) and power supplies are cut off during a wait time of typically 1s. These times are configurable.

TABLE I
NOR FLASH SELECTED DEVICES MAIN CHARACTERISTICS

| Manuf. | Reference | Pack. | Config. | Cap. (Gb) | Acc. Time (ns) | Feat. Size (nm) | Tech. | #Dies |
|---|---|---|---|---|---|---|---|---|
| Micron | PC28F00AM29EW | FBGA 64 | 1024 blks x 64k x 16 bits | 1 | 100 | 65 | FG[a], MLC[b] | 1 |
| Macronix | MX68GL1G0G | FBGA 64 | 2 plns x 512 blks x 64k x 16 bits | 1 | 100 | 55 | FG[a], SLC[c] | 2 |

[a] FG = Floating Gate.
[b] MLC = Multi Level Cell: several bits stored in the same cell.

Each power supply under supervision is monitored independently for SEL detection and processing, however subsequent cut off is performed on all power supplies.
The test board includes also the temperature monitoring of the DUT and beam fluence counter.
The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

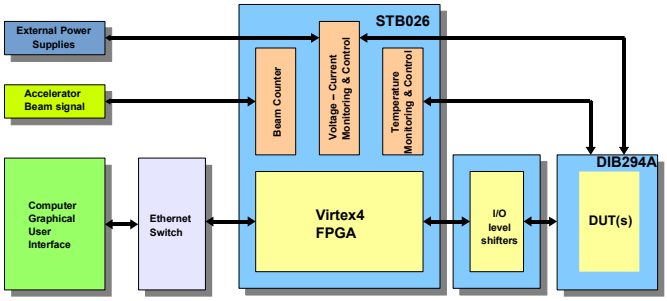


Fig. 1. SEE Test Setup.

## IV. HEAVY ION SEE TEST

### A. Test Conditions

For heavy ion SEE test, material must be removed to enable the heavy ion beam to reach the active area of the die. Therefore, test samples have been opened chemically and tested afterward to be fully functional.

SEU (Single Event Upset) and SEFI (Single Event Functional Interrupt) tests are carried out with power supply at device datasheet minimum recommended value ($V_{DD}$ min = 2.7 V) and at room temperature. On the other hand, SEL tests are carried out with power supply at device datasheet maximum recommended value ($V_{DD}$ max = 3.6 V) and at die temperature of 85 °C.

The samples have been irradiated at RADEF facility located in Jyvaskyla (Finland) using the 9.3 MeV/amu ions cocktail, and HIF facility of UCL university located in Louvain-La-Neuve (Belgium). Target fluence was respectively 1E+06 and 1E+07 ions/cm$^2$ for SEU and SEL tests.

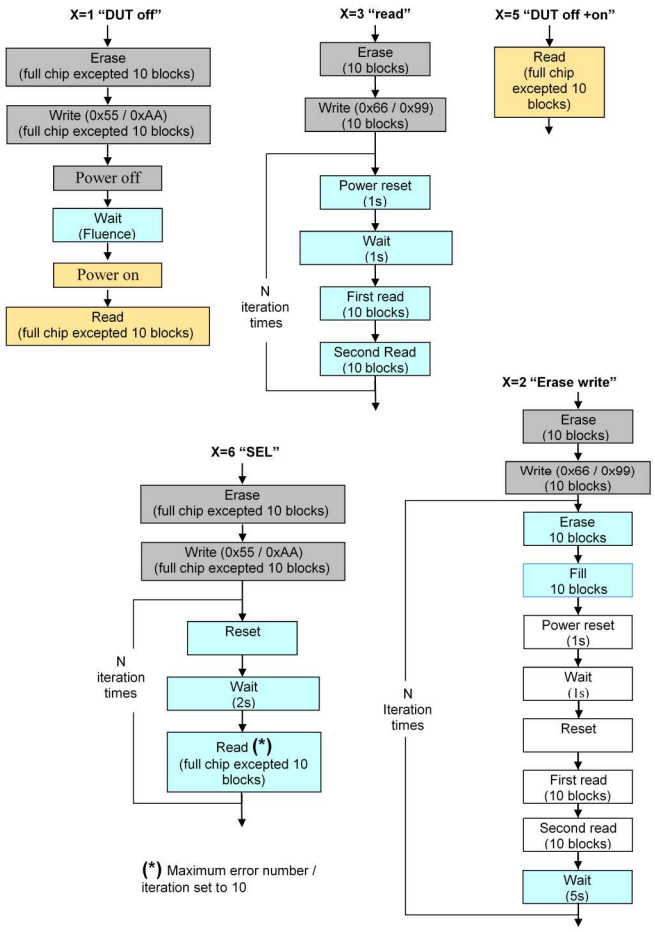


Fig. 2. Heavy Ion SEE Test Sequences.

Test modes and their sequence used during heavy ion SEE tests are summarized in Fig. 2. Operations in grey boxes are performed before the irradiation, those in white are performed with beam OFF (shutter closed), those in blue are performed under irradiation (beam ON), and those in yellow are performed once the beam is stopped at the end of the run.
Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 10 blocks for dynamic behaviour and the rest of the chip for static behaviour. Different patterns are used respectively for dynamic and static tests: 0x99/0x66 for dynamic and 0x55/0xAA for static.

### B. Test Results

NOR flash selected devices showed to be relatively resistant to SEUs with an estimated Weibull saturated cross-section less than 1E–10 cm$^2$/word. However, due to their complex control circuitry and its important associated die logic area which constitute 29% and 21% of total die area, they showed to be sensitive to logic errors (SEFIs) with an estimated Weibull saturated cross-section less than 1E-05 and 2E-05 cm$^2$/device in read and erase/write (E/W) modes respectively. Additionally, erase/write dynamic mode showed to be more sensitive to SEFI with higher saturated cross-section and lower LET threshold (cf. Fig. 5). Moreover, both devices lost completely their

functionality in erase/write dynamic mode under Xenon (62.5 MeV.cm$^2$.mg$^{-1}$), with no recover after power cycling.

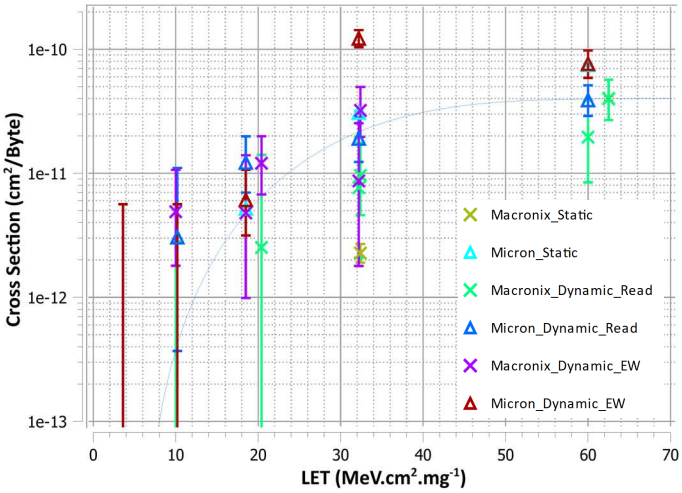


Fig. 3. Heavy ions SEU cross-sections.

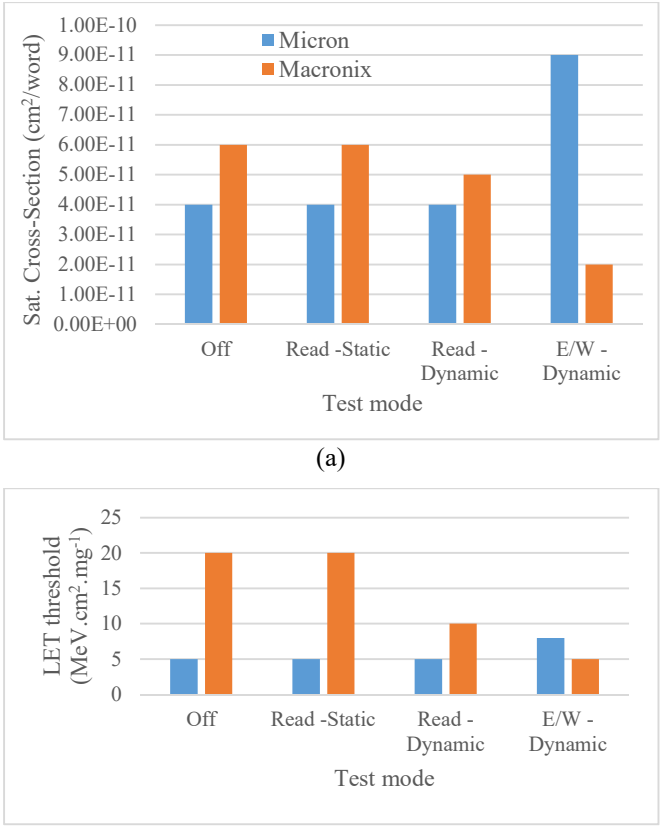


Fig. 4. Heavy ion SEU Weibull estimated saturated cross-section and LET threshold for Micron and Macronix NOR flashs.

Logic errors or SEFIs appeared in the form of:

- Block error corresponding to one or several blocks in error
- Buffer write error corresponding to the entire write buffer (256 words) in error
- Fill error corresponding to buffer write operation exceeding the maximum allocated time of 10 ms
- Erase error corresponding to block erase operation exceeding the maximum allocated time of 4 s

For both devices, the bit error distribution is homogeneous over the word bits, i.e. each bit of the 16 bits forming one word has equal sensitivity. Additionally, the bit flip from 0 to 1, i.e. cell charge loss, is more frequent than bit flip in the opposite direction. It is also very likely that one ion hit can upset more than one word.

**Micron vs Macronix:**

Globally, the Macronix device offered higher LET threshold than Micron (except for SEU in erase/write dynamic test where the two devices are quite similar).

However the two selected parts of NOR flash memories offered similar results for heavy ions SEE tests in terms of saturated cross-section as shown in Fig. 4 and Fig. 5.

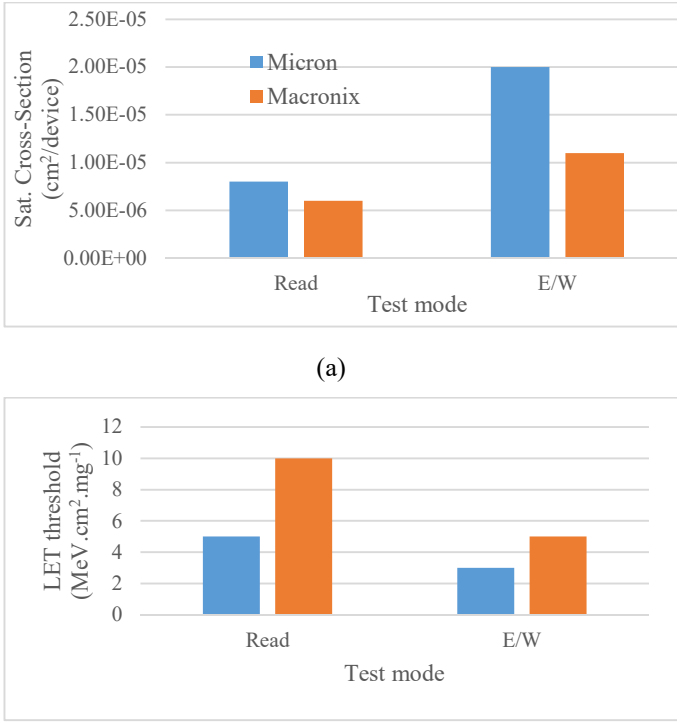


Fig. 5. Heavy ion SEFI Weibull estimated saturated cross-section and LET threshold for Micron and Macronix NOR flashs.

Regarding SEU sensitivity, Macronix offers similar saturated cross-section to Micron but higher LET threshold except for erase/write dynamic mode. Macronix has lower saturation cross-section and LET threshold in dynamic mode in comparison to static mode while the opposite is observed for Micron (cf. Fig. 4).

Regarding SEFI sensitivity, Macronix offers better results than Micron, i.e. lower saturated cross-section and higher LET threshold. Both devices have higher saturated cross-section but lower LET threshold in dynamic mode in comparison to static mode (cf. Fig. 5).

Due to multi-level cell (MLC) technology of Micron device, multiple bit upset (MBU) of size 2 to 6 appeared in addition to single bit upset (SBU), with MBU of size 2 is the most frequent followed by SBU. Furthermore, MBU frequency increases with LET decrease as shown in Fig. 6. At 10.2 MeV.cm$^2$.mg$^{-1}$ more than 90% of SEUs are MBU.

Micron MLC NOR flash device suffers also of many two consecutive bits in error, which may be annoying for error detection and correction scheme. On the other hand, for Macronix, the vast majority (88%) of SEUs are SBU followed by roughly 11% of MBU of size 2 and very few of size 3.

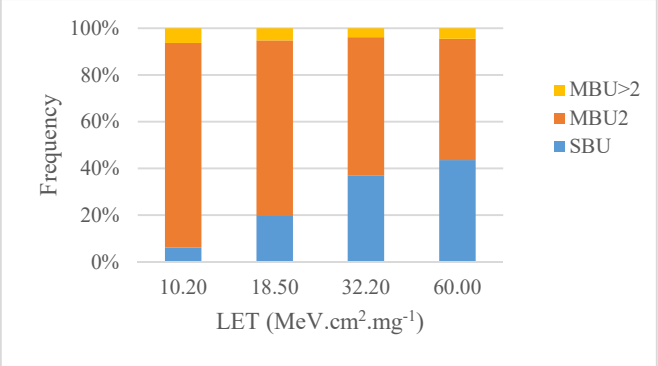


Fig. 6. Frequency of apparition of heavy ion SEUs by type for Micron device in off test mode. SBU is single bit upset, MBU2 is multiple bit upset of size 2, MBU > 2 is MBU of size greater than 2.

As for SELs, NOR flash devices suffered of high current spikes with peak around 0.3 A, and current steps, with corresponding SEL cross sections, at LET of 60 MeV.cm².mg$^{-1}$, below 4E-6 and 5E-4 cm²/device for Micron and Macronix respectively. Furthermore, Macronix device exhibited some SEL events at ambient temperature during dynamic tests under Xenon (60 MeV/mg/cm²).

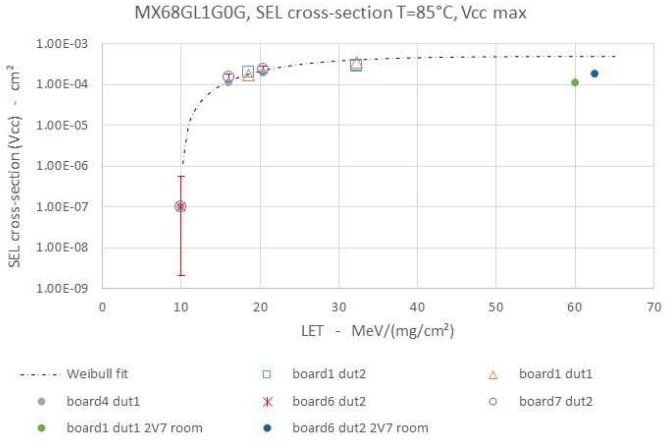


Fig. 7. Heavy ion SEL cross-section plot for Macronix device.

## V. Proton SEE Test

### A. Test Conditions

SEU/SEFI tests are carried out with power supply at device datasheet minimum recommended value ($V_{DD}$ min = 2.7 V) and at room temperature. On the other hand, SEL tests are carried out with power supply at device datasheet maximum recommended value ($V_{DD}$ max = 3.6 V) and at die temperature of 85 °C.

The samples have been irradiated under proton at PIF facility in Villigen, Switzerland [6]. The input energy of the proton beam can vary from few MeVs up to 250 MeV. Then, in irradiation room, local copper degraders can be inserted into the beam to obtain the different user energies. The proton input energy was set to 200 MeV and calibrated. Target fluence was 2E+11 protons/cm$^2$.

Test modes and their sequence used during proton SEE tests are similar to those of heavy ions (cf. Fig. 2). Both static and dynamic results can be extrapolated based on a single run result. This is done by considering 10 blocks for dynamic behaviour and the rest of the chip for static behaviour.

### B. Test Results

NOR flash selected devices showed to be highly resistant to SEUs (cell errors) and SEFIs (logic errors) under proton irradiation with only very few errors detected during only erase/write sequence for both Micron and Macronix devices. Errors consist in very few cell errors (SEUs only) with corresponding cross-section below 2.3E-16 cm$^2$/word, and very few logic errors (buffer write error, fill error, and erase error) with corresponding cross-section below 2.0E-11 cm$^2$/device.

As for SELs, NOR flash devices did not exhibit neither latch-up event nor current steps under proton irradiation.

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