2022 22nd European Conference on Radiation and Its Effects on Components and Systems (RADECS) | 979-8-3503-7123-9/22/$31.00 ©2022 IEEE | DOI: 10.1109/RADECS55911.2022.10412562

Compendium of SEE and TID Test Results for DDR4 SDRAM memories

Arnaud Dufour[1], Jérôme Carron[1], David Dangla[1], Florence Malou[1], Julien Mekki[1], Bendy Tanios[2], Gabriel Durán Cárdenas[2], Benjamin Crouzat[2], Francois-Xavier Guerre[2], Aomer Ait-Ali-Said[3]

***Abstract*— This paper reports the results and analysis of single event effects (SEE) tests and total ionizing dose (TID) on DDR4-SDRAM memories. The compendium covers five DDR4-SDRAM references from different manufactures tested in the frame of CNES studies.**

***Keywords*— Single Event Effects, Total Ionizing Dose, Components, Memories, SDRAM, DDR4**

I. INTRODUCTION

Our world is changing fast! This is fascinating for some people, frightening for others. Space is no exception as is in full mutation. Indeed, international competition between major power and private sector initiatives to make access to space less expensive are as many upheavals as new challenges to be taken up for flying system designers in order to guarantee the highest levels of performance without scarifying too much the overall reliability.

Space data becomes the center of interest. We need fast, precise, and instantaneous information coming from everywhere, anytime. The days of passive satellites are over, and an ever-increasing part of the processing is now done on-board to overcome downlink limitations, as the goal is to maximize useful data transmission through the same bandwidth. This implies the use of very powerful microprocessors, reprogrammable devices or SoCs (System on Chip) coupled with the fastest working memories available on the market.

Successive generations of SDRAM (Synchronous Dynamic Random Access Memory) memories with DDR (Double Data Rate) interface have made personal desktop computer and smartphone performances stronger, their usage in space on-board computer appeared as an evidence. However, as rad-hard derivatives of this type of memories are not available, commercial-off-the-shelf (COTS) components are used. For that reason, SEE (Single Event Effect) and TID (Total Ionizing Dose) testing are required in order to guarantee their proper operation during a space mission.

Following the work done on the previous period, the aim of this paper is to present a summary of the SEE and TID tests performed on five DDR4-SDRAM references from different manufacturers in the frame of CNES studies. Alter conducted these experiments on the past three years for SEE tests and TRAD for TID tests.

II. IRRADIATION FACILITIES

A. *SEE Test Facilities : RADEF*

The RADEF facility[1] includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis. The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions.
The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices.

B. *TID Test Facilities : GAMRAY*

GAMRAY facility[2] is a panoramic irradiation room for TID testing. Gamma irradiation are performed with Cobalt 60 source of 14.8 TBq (04/09/2015) with energies of 1.17 MeV and 1.33 MeV.
The useful irradiation volume is about 45 m^3. The Gamma ray beam dose rate is from 10 rad/h to 4 krad/h (3 mrad/s to 1 rad/s) [1].
The dosimetry measurement methodology of the gamma radiation laboratory, is accredited by COFRAC, according to the international standard ISO / IEC 17025.

III. EXPERIMENTAL TEST SETUP

A. *Selected components*

At CNES level, we selected several references listed in TABLE I that was available on the market and also fitted our needs.

[1]Arnaud Dufour, Jérôme Carron, David Dangla, Florence Malou are with CNES Toulouse, France (email : firstname.name@cnes.fr)

[2]Bendy Tanios, Gabriel Duran are with Alter France, Toulouse, France (email : B.Tanios@altertechnology.fr)

[1]Aomer Ait-Ali-Said is with TRAD, Labège, France, (email : aomer.ait-ali-said@trad.fr)

TABLE I
LIST OF TESTED DDR4-SDRAM REFERENCES

Reference	Function	Manufacturer
MT40A256M16LY-062E IT:F	DDR4 4Gbit (x16)	Micron
K4A4G165WE-BITD (CL19)	DDR4 4Gbit (x16)	Samsung
H5AN8G6NCJR-VKI	DDR4 8Gbit (x16)	Hynix
NT5AD256M16D4-HRI (CL19)	DDR4 4Gbit (x16)	Nanya
MT40A512M16JY-075E AIT:B	DDR4 8Gbit (x16)	Micron

B. *SEE Test bench description*

The test system is based on a Kintex Ultrascale+ FPGA from Xilinx (cf. Fig. 1). The Test Bench is controlled in real time by a master computer via Ethernet protocol. The computer acts as the head master, and can modify the settings as well as the test sequence on the fly, if necessary. All the test data are sent to the computer and recorded on its hard drive.

The STB033A board (cf. Fig. 2) includes 2 slots for DDR4 SO-DIMM daughter boards that can be used up to 2666 MTPS operating speed. In addition to standard operations like write, read and refresh, our custom memory controller includes a potential SEFI mitigation technique that showed in the past to be effective for DDR3 devices [3]. It consists in resetting and reinitializing the DDR4 devices.

The supervisor board performs biasing, functional checks, voltage/current monitoring and latch-up management of the DUT power supplies with up to 8 independent channels.

The communication between the test chamber and the controlling computer is effectively done by a 100 Mbit/s Ethernet link which safely enables high speed data transfer.

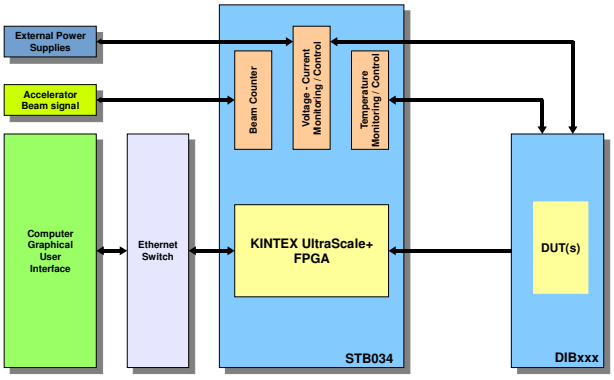

Fig. 1 Alter France SEE test setup for DDR4 SDRAM memories

SEU (Single Event Upset) / SEFI (Single Event Functional Interrupt) tests were carried out with power supply close to device datasheet recommended value (V_{DD} nom) and room temperature. SEL (Single Event Latchup) tests were carried out with power supply at device maximum allowed value (V_{DD} max) and at the maximum operating temperature.

Fig. 2 SEE test board STB033A for DDR4 SDRAM memories

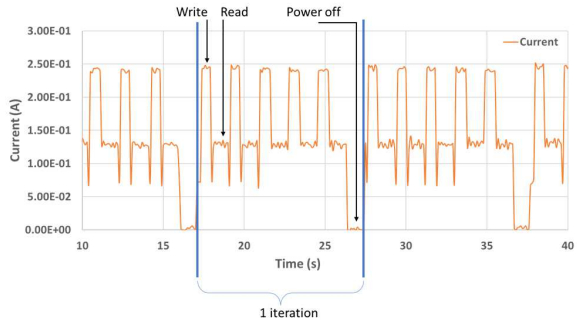

Fig. 3 DUT current during dynamic test

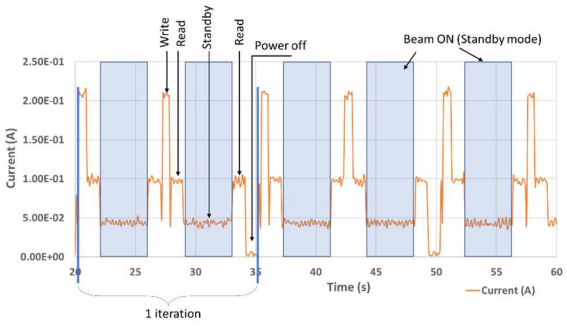

Fig. 4 DUT current during static test

Devices are tested at their maximum operating speed (DDR4-2666=1333MHz). Two different test modes were applied:

- Dynamic mode: All operations (write, read, etc) are performed under beam, as shown on Fig. 3.
- Static mode: The DUT is irradiated only when it is in standby mode, as shown in blue on Fig. 4. All other operations like write, read, reset, power cycling, etc. are performed out of beam using a beam shutter. Periodic reset and/or power cycling permits to avoid too-long SEFIs. [4]

C. *Sample preparation*

All part types were flip-chip mounted on commercial SODIMMs boards. Each DUT has been prepared by epoxy

removal and die back thinning down to about 75µm, to allow the RADEF heavy ion beam to reach the active area of the die. The maximum thickness was 80µm with a thickness uniformity of +/- 5 µm.

D. *TID Test bench description*

For TID, the DUTs were tested using a DDR4 tester using a custom SODIMM adapter. This tester is capable to check functional test pattern and detect failures using a different read write algorithms, comparisons and repetitive read test pattern.
For all runs, supply currents were measured with I/O pins in static mode and 14 functional tests patterns were performed at 1333Mhz frequency and at 2.5V for V_{DD}, V_{DDQ} supply voltage and at 1.2 V for Vpp .[5]

IV. Tests Results and Discussion

As this paper is a summary of test results, only the key information about the tests is reported. Consequently, it is recommended to contact the paper's authors for detailed information. Abbreviations and conventions used are listed in table II, all the acronyms are listed in Table III.

TABLE II
UNITS FOR PROPERTIES

SYMBOL	METRICS
LET_{th}	MeV.cm²/mg
σ_{Sat}	cm²/device
$\sigma_{Sat/bit}$	cm²/bit
E_{th}	MeV
DR	RAD/H

TABLE III
ACRONYMS

ACRONYM	DEFINITION
DUT	*Device under test*
LETTH	*Linear Energy Transfer Threshold*
MBU	*Multi-Bit Upset*
MBU-2	*Multi-Bit Upsets with 2 error bits*
MBU-3	*Multi-Bit Upsets with 3 error bits*
MBU>3	*Number of words containing more than 3 error bits*
SBU	*Single Bit Upset*
SEL	*Single Event Latch up*
SEU	*Single Event Upset*
SEFI	*Single Event Functional Interruption*
TID	*Total Ionizing Dose*
DC	*Date Code*
DR	*Dose Rate*
PF	*Parametric failure*
FF	*Functional Failure*
LE	*Logic Errors*

A. *MT40A256M16LY-062E IT:F from Micron*

1) Single Event Latchup results

SEL tests were performed at high temperature (95°C), $1x10^7$ ions/cm² fluence and maximum operating voltage. During the SEL tests, the memory is used by "write-write-read" cycles.
No SEL was detected up to a LET of 60 MeV.cm².mg^{-1}.
Nevertheless, the nominal consumption is quite high (around 200 mA for VDD, see Fig. 5, and 100 mA for Vpp). At the beginning of each run, the power consumption is low, and as soon as the beam is on with a flux of 2.5E+04 ions/s/cm² , the current reaches high values.

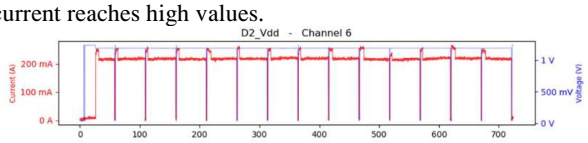

Fig. 5 High consumption observed on Vdd line

2) Single Event Upset results

SEU tests were performed at room temperature on two DUT (see Fig. 6). First word errors were detected during both Dynamic and Static testing modes at a LET of 8.3MeV.cm².mg^{-1}. This reference has a very low sensitivity regarding MBU (only one detected on 1 DUT at Xenon). Between dynamic and static tests mode, a high resemblance in the behavior have been seen.

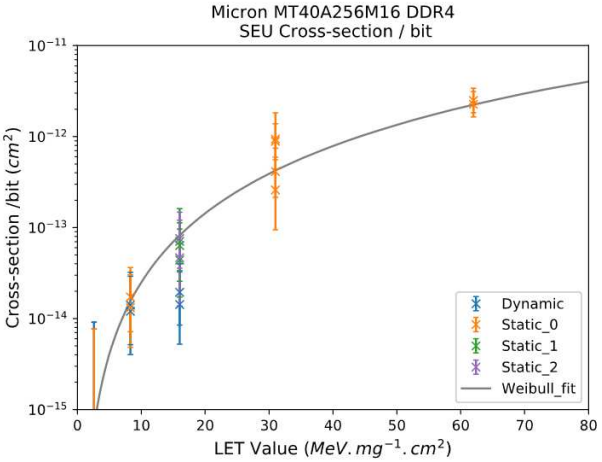

Fig. 6 SEU cross section during static and dynamic modes

TABLE IV
WEIBULL FIT FOR SEU STATIC AND DYNAMIC MODES

Test mode	LETth [MeV.cm².mg^{-1}]	Saturation [cm².bit^{-1}]
Static	0.5	2.6E-11
Dynamic	0.5	2.6E-11

3) Logic Errors

During SEU tests, row, column and Single Event Functional Interrupt (SEFI) errors were detected and accounted as "Logic Errors". These errors are summarized in TABLE V.
Logic Errors were detected for all LETs (starting from 2.6 MeV.cm².mg^{-1}).

TABLE V
A. MT40A256M16LY LOGIC ERRORS SUMMARY

Test Mode	Ion	LET @75µm [MeV.cm².bit⁻¹]	ON Fluence [ions.cm⁻²]	Rows errors	Columns errors	SEFIs	Total logic errors		
							Mean	Lower bound 95% CI	Upper bound 95% CI
Dynamic	Fe	16	1.87E+06	6	9	64	79	63	98
Static	Xe	62	1.36E+5	5	0	85	90	72	110

4) Stuck bits

Stuck bits were observed before and after each run on different test samples. No stuck bit measurement were done in the middle of the runs.

Some stuck bits were observed under the beam. The LET threshold is between 8.3 and 16 MeV.cm².mg^{-1}. The quantity of stuck bits observed is very low and all of them except one recovered very quickly (at least before the next run). We can assume that the probability of occurrence is higher than what we observed due to their fast recovery time.

5) Total Ionizing Dose results

The total dose steady-state irradiation test using gamma rays from Cobalt 60 source has been carried out on 10 MT40A256M16LY-062E up to 100 krads (Si) at a low dose rate of 180 rad/h. Irradiations were performed at room temperature and five DUTs were biased in static mode and five were grounded (Fig. 7).

No failure or significant drifts observed on the DUTs at total dose level.

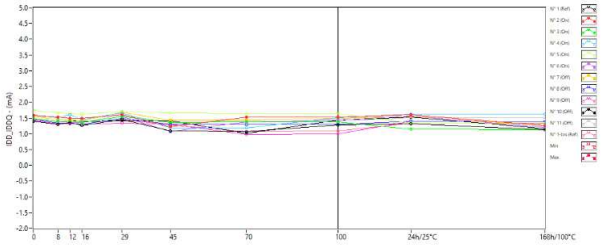

Fig. 7 MT40A256M16LY-062E – IDD_IDDQ parameter as function of TID

B. *K4A4G165WF-BITD from Samsung*

K4A4G165WF is a 4Gbit (x16) DDR4 SDRAM memory.

1) Single Event Latchup results

SEL tests were performed at high temperature (125°C), 1E+07 ions/cm² fluence and maximum operating voltage. During the SEL tests, the memory is used by "write-write-read" cycles.

No SEL was detected up to a LET of 60 MeV.cm².mg^{-1}. No overconsumption observed during runs.

2) Single Event Upset results

SEU tests were performed at room temperature. SBU were detected during both Dynamic and Static testing modes at a minimum LET of 2.6 MeV.cm².mg^{-1}(cf Fig. 8). MBU were detected during both Dynamic and Static testing modes at a minimum LET of 8.3 MeV.cm².mg^{-1}.

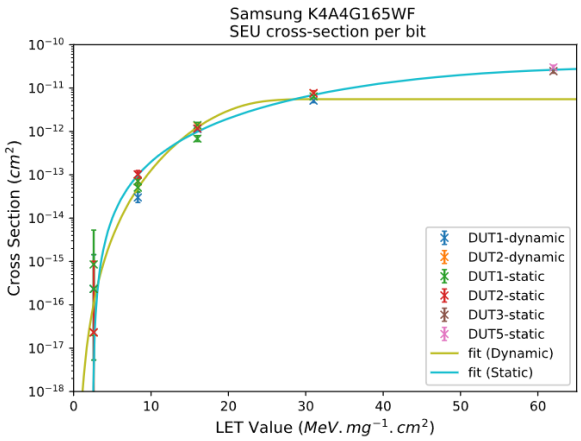

Fig. 8 Comparison of SEU cross-section per bit for Dynamic and Static modes (K4A4G165WF-BITD)

TABLE VI
WEIBULL FIT FOR SEU STATIC AND DYNAMIC MODES

Test mode	LETth [MeV.cm².mg⁻¹]	Saturation [cm².bit⁻¹]
Static	2.5	3.1E-11
Dynamic	0.2	8.9E-13

3) Logic Errors

During SEU tests, row, column and Single Event Functional Interrupt (SEFI) errors were detected and accounted as "Logic Errors". These errors are summarized in TABLE VII.

Logic Errors were detected for all LETs (starting from 2.6 MeV.cm².mg^{-1}).

TABLE VII
K4A4G165WF-BITD LOGIC ERRORS SUMMARY AT XENON

Test Mode	Ion	LET @75µm [MeV.cm².bit⁻¹]	ON Fluence [ions.cm⁻²]	Rows errors	Columns errors	SEFIs	Total logic errors		
							Mean	Lower bound 95% CI	Upper bound 95% CI
Dynamic	Kr	31	1.2E+06	52	31	7	84	67	103
Static	Xe	60.88	4.6E+05	0	0	3	3	1	9

4) Stuck bits

Stuck bits were observed before and after each run on different test samples. No stuck bit measurement were done in the middle of the runs.

Lots of stuck bits were observed under the beam. The LET threshold is between 2.6 and 8.3 MeV.cm².mg^{-1}. The quantity of stuck bits observed increases as the energy is higher. The recovery time is very long as we never recovers all the memory, even at low energy. Today we cannot conclude on the maximum retention time of the stuck bit on this reference.

5) Total Ionizing Dose results

We did not performed TID tests on this reference as the behavior against stuck bits was not satisfactory.

C. *H5AN8G6NCJR-VKI from Hynix*

H5AN8G6NCJR is a 8Gbit (x16) DDR4 SDRAM memory.

1) Single Event Latchup results

SEL tests are performed at high temperature (125°C), a 1.0.107 ions/cm² fluence and a VDD max power supply. No SEL was detected up to a LET of 60 MeV/mg/cm. No overconsumption observed during runs.

2) Single Event Upset results

SEU tests were performed at room temperature, with a minimum of 1E+06 ions/cm² fluence. SBU were detected during both Dynamic and Static testing modes at a LET of 2.6 MeV.cm².mg^{-1} (cf Fig. 9). MBU were detected during both Dynamic and Static testing modes at a LET of 8.3 MeV.cm².mg^{-1}.

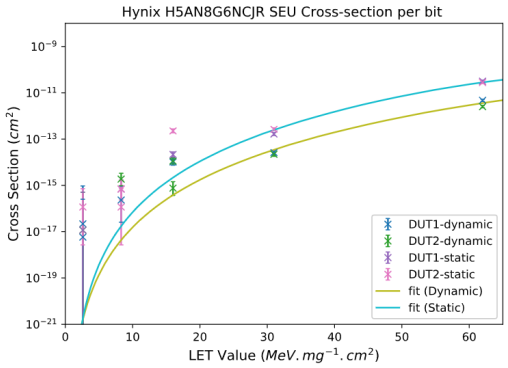

Fig. 9 Comparison of SEU cross-section per bit for Dynamic and Static modes (H5AN8G6NCJR-VKI)

TABLE VIII
WEIBULL FIT FOR STATIC AND DYNAMIC MODES

Test mode	LETth [MeV.cm².mg^{-1}]	Saturation [cm².bit^{-1}]
Static	0.5	8.5E-11
Dynamic	0.5	2.3E-11

3) Logic Errors

During SEU tests, row, column and Single Event Functional Interrupt (SEFI) errors were detected and accounted as "Logic Errors". These errors are summarized in TABLE IX.

Logic Errors were detected for all LETs (starting from 8.3 MeV.cm².mg^{-1}).

TABLE IX
H5AN8G6NCJR LOGIC ERRORS SUMMARY AT XENON

Test Mode	Ion	LET @75µm [MeV.cm².bit^{-1}]	ON Fluence [ions.cm^{-2}]	Rows errors	Columns errors	SEFIs	Total logic errors		
							Mean	Lower bound 95% CI	Upper bound 95% CI
Dynamic	Xe	62	1.6^{E}+06	55	8	12	75	59	94
Static	Xe	62	1.7^{E}+06	268	44	4	320	286	357

4) Stuck bits

Stuck bits were observed before and after each run on different test samples. No stuck bit measurement were done in the middle of the runs.

Lots of stuck bits were observed under the beam. The LET threshold is between 8.3 and 16 MeV.cm².mg^{-1}. The quantity of stuck bits observed for energies between 8.3 MeV.cm².mg^{-1} and 31 MeV.cm².mg^{-1} is very low and all of them recovered very quickly (at least before the next run). We can assume that the probability of occurrence is higher than what we observed due to their fast recovery time.

At 62 MeV.cm².mg^{-1} the probability of occurrence is significantly higher and the recovery time is longer. In the worst case, around 2205 stuck bits appeared during a run at a fluence of 2E+06 ions.cm^{-2}.

Today we did not conclude on the maximum retention time of the stuck bit with 62MeV.cm²/mg LET.

5) Total Ionizing Dose results

The total dose steady-state irradiation test using gamma rays from Cobalt 60 source has been carried out on 10 H5AN8G6NCJR up to 100 krads (Si) at a low dose rate of 180 rad/h. Irradiations were performed at room temperature and five DUTs were biased in static mode and five were grounded (Fig. 10).

No failure or significant drifts observed on the DUTs at total dose level.

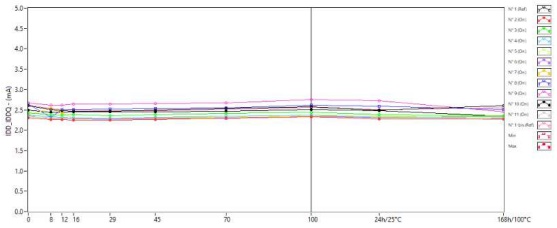

Fig. 10 H5AN8G6NCJR-VKI – IDD_IDDQ parameter as function of TID

D. *NT5AD256M16D4-HRI from Nanya*

NT5AD256M16D4 is a 4Gbit (x16) DDR4 SDRAM memory.

1) Single Event Latchup results

SEL tests are performed at high temperature (95°C), a 5E+06 ions/cm² fluence and a VDD max power supply.
No SEL was detected up to a LET of 62 MeV/mg/cm.
However, Current steps were identified for Vdd and Vpp, as high as 100mA, and the power consumption even reaches 300 mA (see Fig. 11) . The functionality of the DUT was confirmed for a DUT after the SEL run, so the current steps did not have a destructive effect on the sample.

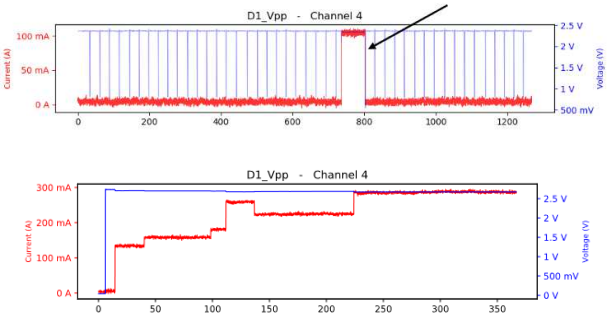

Fig. 11 NT5AD256M16D4-HRI step current increases under Xenon

2) Single Event Upset results

Runs were performed at and room temperature and nominal power supply.
Two DUTs were tested and showed SEU from a LET of 8.2 MeV.cm².mg^{-1} both in static and dynamic mode. Effective fluences are lower than the received fluences due to the power pulses and other considerations of the test sequences were part of the ions do not have an impact on the cross-sections.
No MBU was observed.
Static and dynamic modes are quite similar as seen on Fig. 12:

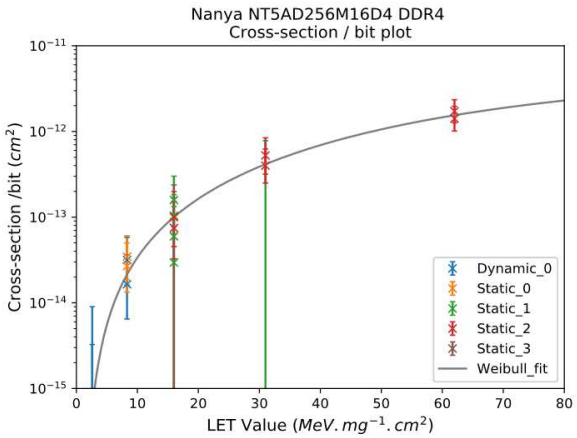

Fig. 12 Comparison of upset cross-section per bit for Dynamic and Static modes (NT5AD256M16D4-HRI)

TABLE X
WEIBULL FIT FOR STATIC AND DYNAMIC MODES

Test mode	LETth [MeV.cm².mg^{-1}]	Saturation [cm².bit^{-1}]
Static	1.45	4.4E-12
Dynamic	1.45	4.4E-12

3) Logic Errors

During SEU tests, row, column and Single Event Functional Interrupt (SEFI) errors were detected and accounted as "Logic Errors". These errors are summarized in TABLE XI.
Logic Errors were detected for all LETs (starting from 2.6 MeV.cm².mg^{-1}).

TABLE XI
NT5AD256M16D4 LOGIC ERRORS SUMMARY AT XENON

Test Mode	Ion	LET @75µm	ON Fluence [ions.cm^{-2}]	Rows errors	Columns errors	SEFIs	Total logic errors		
							Mean	Lower bound 95% CI	Upper bound 95% CI
Dynamic	Ar	8	1.78^{E}+06	340	70	5	184	158	213
Static	Xe	62	2^{E}+05	62	11	3	77	61	96

4) Stuck bits

Stuck bits were observed before and after each run on different test samples. No stuck bit measurement were done in the middle of the runs.
Lots of stuck bits were observed under the beam. The LET threshold is between 2.6 and 8.3 MeV.cm².mg^{-1}. The quantity of stuck bits observed for energies between 8.3 MeV.cm².mg^{-1} and 62 MeV.cm².mg^{-1} is very low and all of them recovered very quickly (at least before the next run). We can assume that the probability of occurrence is higher than what we observed due to their fast recovery time.

5) Total Ionizing Dose results

The total dose steady-state irradiation test using gamma rays from Cobalt 60 source has been carried out on 10 NT5AD256M16D4-HRI up to 99 krads (Si) at a low dose rate of 180 rad/h. Irradiations were performed at room temperature and five DUTs were biased in static mode and five were grounded (Fig. 13).
No failure observed on the DUTs at total dose level. Only a drift of the IPP current was observed on all the parts biased ON at 99 krad step.
These parts recovered after the last annealing (168 hours at 100°C)

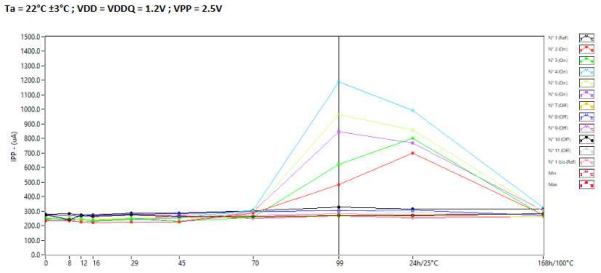

Fig. 13 NT5AD256M16D4-HRI – IPP parameter as function of TID

E. *MT40A512M16JY-075E AIT:B from Micron*

MT40A512M16 is 8Gbit (x16) DDR4 SDRAM memory.

1) Single Event Latchup results

SEL tests were performed at high temperature (95°C), $1x10^7$ ions/cm² fluence and maximum operating voltage on three devices. During the SEL tests, the memory is used by "write-write-read" cycles.

No SEL was detected up to a LET of 60 MeV.cm².mg^{-1}.

Nevertheless, step current increases have been observed using Xenon ions as shown on Fig. 14. These events were probably linked to internal SEFI and were not pure SELs as they do not heal without external intervention (manual switch OFF/ON).

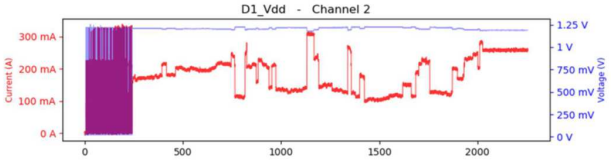

Fig. 14 MT40A512M16 step current increases under Xenon

2) Single Event Upset results

SEU tests were performed at room temperature, with a $1x10^6$ ions/cm² fluence. Word errors were detected during both Dynamic and Static testing modes. The memory has a total 536 870 912 words, i.e. 8 589 934 592 bits and LET values ranged from 2.6 to 60.88 MeV.cm².mg^{-1}. Two DUTs were tested, showing sensitivity from 2.6 MeV.cm².mg^{-1} and both Single Bit and Multi-Bit Errors. The results are quite homogenous between the two tested parts. Fig. 15 shows the cross-section and Weibull fit for both dynamic and static test modes.

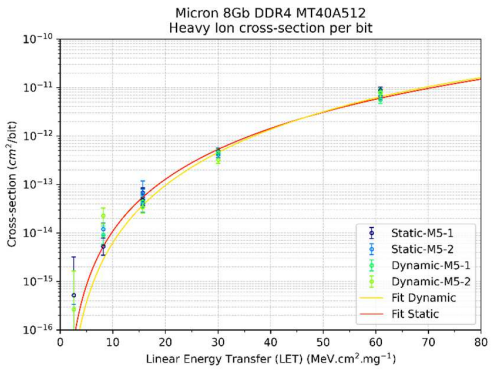

Fig. 15 Comparison of upset cross-section per bit for Dynamic and Static modes (Micron MT40A512M16)

The TABLE XII summarizes the LET threshold and asymptotic cross-section saturation for these Weibull fits. Both fits are very similar.

TABLE XII

WEIBULL FIT FOR STATIC AND DYNAMIC MODES

Test mode	LETth [MeV.cm².mg^{-1}]	Saturation [cm².bit^{-1}]
Static	0.5	1.14E-10
Dynamic	0.5	4.49E-11

3) Logic Errors (LE)

During SEU tests, row, column and Single Event Functional Interrupt (SEFI) errors were detected and accounted as "Logic Errors". These errors are summarized in TABLE XIII.

Logic Errors were detected for all LETs (starting from 2.6 MeV.cm².mg^{-1}).

TABLE XIII

MT40A512M16 LOGIC ERRORS SUMMARY AT XENON

Test Mode	Ion	LET @75µm [MeV.cm².bit^{-1}]	ON Fluence [ions.cm^{-2}]	Rows errors	Columns errors	SEFIs	Total logic errors		
							Mean	Lower bound 95% CI	Upper bound 95% CI
Dynamic	Xe	60.88	1.02E+06	1	5	28	34	24	48
Static	Xe	60.88	9.71E+05	2	3	19	24	16	36

4) Stuck bits

Stuck bits were observed before and after each run on different test samples. No stuck bit measurement were done in the middle of the runs.

Some stuck bits were observed under the beam. The LET threshold was about 2.6 MeV.cm².mg^{-1}. The quantity of stuck bits observed for energies between 2.6 MeV.cm².mg^{-1} and 30.06 MeV.cm².mg^{-1} is very low and all of them recovered very quickly (at least before the next run). We can assume that the probability of occurrence is higher than what we observed due to their fast recovery time.

At 60.88 MeV.cm².mg^{-1} the probability of occurrence is significantly higher and the recovery time is longer. In the worst case, around 40 stuck bits appeared during a run at a fluence of 2.88E+04 ions.cm^{-2}.

Today we did not conclude on the maximum retention time of the stuck bit with 60.88MeV.cm²/mg LET.

5) Total Ionizing Dose results

The total dose steady-state irradiation test using gamma rays from Cobalt 60 source has been carried out on 10 MT40A512M16JY-075E up to 99 krads (Si) at a low dose rate of 180 rad/h. Irradiations were performed at room temperature and five DUTs were biased in static mode and five were grounded (Fig. 16).

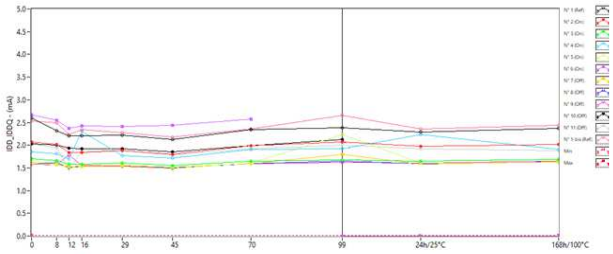

Fig. 16 MT40A512M16 – IDD_IDDQ parameter as function of TID

Due to overconsumption, Part no.6 was not measurable at 99 krad (Si) step. Part no.10 was damaged during insertion into the socket of DDR4 test bench at annealing step. The part was broken and was removed from the lot.
For the others, all parameters are within specifications and no failure was observed at total dose level for all other parts biased ON. After 168h annealing, part no.6 was still in failure. All parameters are within specifications and no failure was observed at total dose level for parts biased OFF (see TABLE XIV).

TABLE XIV
MT40A512M16 - REPETITIVE READ TEST PATTERN AS FUNCTION OF TID

	Dose (krad (Si))								Annealing	
	0	8	12	16	29	45	70	99	24h/25°C	168h/100°C
N° 1 (Ref)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 2 (On)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 3 (On)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 4 (On)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 5 (On)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 6 (On)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL*	FAIL*	FAIL*
N° 7 (OFF)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 8 (OFF)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 9 (OFF)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 10 (OFF)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	N/A**	N/A**	N/A**
N° 11 (OFF)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
N° 1-bis (Ref)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

V. Conclusion

We have presented recent data from SEE and TID tests on DDR4 SDRAM memories selected to be candidate on space missions. The compendium includes 5 references. It is recommended to use the data presented here with caution (not a full test report) and to contact the authors for more details on a specific part results.

References

[1] [RADEF]. https://www.jyu.fi/fysiikka/en/research/accelerator/radef
[2] [GAMRAY]. http://www.trad.fr/GAMRAY-Co60-Irradiation-Facility-118.html?lang=en
[3] B. Tanios, F. Lochon, O. Perrotin, P. Fontana, B. Forgerit, F. Tilhac, F.X. Guerre and C. Poivey., "Radiation Effects (Single Event Effects and Total Ionization Dose) on Commercial LP-DDR3 SDRAM for ESA JUICE Mission" in *RADECS2019,* Montpellier, France, 2019.
[4] Single Event effects test methods and guidelines - ESCC Basic Specification No 25100
[5] Total Dose Steady-State Irradiation Test Method - ESCC Basic Specification No. 22900